Faculty of Electronic and Computer Engineering

STATISTICAL MODELLING AND OPTIMIZATION OF INPUT PROCESS PARAMETERS VARIATIONS IN SILICON-ON-INSULATOR MOSFET DEVICE

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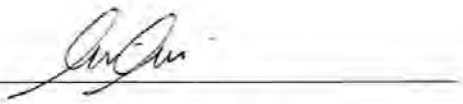
DECLARATION

I declare that this thesis entitles "Statistical modelling and Optimization of Input Process parameters Variations in Silicon-on-insulator MOSFET device" is the result of my own research except as cited in the references. The thesis has not been accepted for any degree and is not concurrently submitted in candidature of any other degree.

Signature : 

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APPROVAL

I hereby declare that I have read this thesis and in my opinion, this thesis is sufficient in terms of scope and quality for the award of Master of Science in Electronic Engineering.

Signature : _____

Name : DR. FAUZIYAH BINTI SALEHUDDIN

Date : 16 NOVEMBER 2017.

DEDICATION

To my beloved mother and father

ABSTRACT

The steady miniaturization of the conventional (planar bulk) Metal Oxide Semiconductor Field Effect Transistor (MOSFET) has been effective in providing continual improvements in integrated circuit performance. However, increased leakage current and variability in transistor performance are the major challenges for continued scaling of bulk-Si MOSFET technology. Therefore, Silicon-on-insulator (SOI) technology has been recognized as an effective approach to mitigate the short-channel effect (SCE) problems. SOI technology allows optimum electrical characteristics to be obtained for low power and high performance circuits. In this research, the impact of the process parameters such as halo implantation energy, halo implantation dose, Source/Drain implantation Dose, and Source/Drain (S/D) implantation energy on the response characteristics for the NMOS and PMOS SOI MOSFET devices were investigated. The virtual fabrication of the device was performed using ANTHENA module while the device electrical characteristics were simulated using ATLAS module. ANTHENA and ATLAS are the modules contained in Silvaco TCAD software. These two modules were combined with an appropriate statistical method to aid in designing and optimizing the process parameters. In the optimization of the process parameter variations towards the multiple device's characteristics of SOI MOSFET devices, Taguchi method and 2k factorial designs were used. The performance between these two methods in the NMOS and PMOS SOI MOSFET device was evaluated. Based on the observation, it was found that the results given by the Taguchi method were more accurate than 2k Factorial designs due to the presence of noise factors. In PMOS device, the most dominant or significant factors for S/N Ratio were Halo implantation dose and S/D implantation energy. While the S/N Ratio values after the optimization approach for V_{TH}, SS, I_{OFF} and I_{ON} were 91.27dB, -39.37dB, 335.68dB and -80.16dB respectively. Meanwhile, for NMOS, the most dominant or significant factor for S/N Ratio was S/D implantation energy. The S/N ratio values after the optimization approach for V_{TH}, SS, I_{OFF} and I_{ON} were 53.64dB, -38.60dB, 234.86dB and 54.70dB respectively. All these values were within the predicted range. In PMOS device, the results showed that the V_{TH}, SS, I_{OFF} and I_{ON} after optimization approaches were -0.573V, 92.95mV/dec, 26.04×10^{-18}A/μm and 98.19μA/μm respectively. For NMOS device, the values of V_{TH}, SS, I_{OFF} and I_{ON} after optimization approaches were +0.546V, 85.08mV/dec, 2.034pA/μm and 344.17μA/μm respectively. Most of the results obtained were within the range and met the requirement of low power (LP) technology for the year 2016 as predicted by International Technology Roadmap for Semiconductor (ITRS) 2013. As a conclusion, the design of NMOS and PMOS SOI MOSFET has successfully been created and through the Taguchi method, the optimal solution for the robust design of the devices has successfully been achieved.

ABSTRAK

Proses pengecilan saiz yang stabil untuk konvensional Transistor Kesan Medan Logam-Oksida-Semikonduktor (MOSFET) dengan jayanya telah memberi cara yang berkesan dalam memastikan peningkatan prestasi dalam litar bersepadu. Namun demikian, peningkatan masalah arus bocor serta kebolehubahan dalam prestasi transistor adalah masalah paling mencabar dalam usaha mengecilkan teknologi MOSFET. Oleh itu, Silikon di atas Penebat (SOI) telah dikenali sebagai salah satu cara menghalang dari masalah kesan salur pendek (SCE). Teknologi SOI membolehkan ciri elektrik yang optimum dapat diperolehi untuk litar kuasa rendah dan berprestasi tinggi. Dalam kajian ini, kesan parameter proses seperti tenaga implantasi halo, dos implantasi halo, dos implantasi punca/salir dan juga tenaga implantasi punca/salir terhadap ciri-ciri NMOS and PMOS SOI MOSFET telah diselidik. Fabrikasi maya bagi peranti ini telah disimulasikan menggunakan modul ATHENA manakala bagi ciri elektrik, peranti dijalankan menggunakan modul ATLAS. Modul ATHENA dan ATLAS ini adalah modul yang terkandung didalam perisian Silvaco TCAD. Kedua-dua modul ini digabungkan dengan kaedah statistikal yang sesuai untuk membantu mereka bentuk serta mengoptimumkan parameter proses. Bagi membolehkan variasi parameter proses yang optimum dijalankan terhadap pelbagai ciri elektrik untuk peranti SOI MOSFET, reka bentuk kaedah Taguchi dan 2k-factorial telah digunakan. Prestasi antara kedua-dua kaedah dalam peranti NMOS dan PMOS SOI MOSFET telah dinilai. Berdasarkan pada pemerhatian, didapati bahawa keputusan yang diberikan oleh kaedah Taguchi adalah lebih tepat daripada reka bentuk 2k-factorial disebabkan kehadiran faktor hingar. Didalam peranti PMOS, faktor yang paling dominan atau paling ketara bagi nisbah S/N ialah dos implantasi halo dan tenaga implantasi S/D. Nilai nisbah S/N selepas dioptimumkan bagi V_{TH}, SS, I_{OFF} dan I_{ON} adalah 91.27dB, -39.37dB, 335.68dB dan -80.16dB masing-masing. Untuk peranti NMOS pula, faktor yang paling dominan atau paling ketara bagi nisbah S/N adalah faktor tenaga implantasi S/D. Nilai nisbah S/N bagi V_{TH}, SS, I_{OFF} dan I_{ON} selepas dioptimumkan adalah 53.64dB, -38.60dB, 234.86dB dan 54.70dB masing-masing. Semua nilai yang telah dioptimumkan berada didalam julat yang diramalkan. Didalam peranti PMOS, keputusan V_{TH}, SS, I_{OFF} dan I_{ON} selepas dioptimumkan menunjukkan nilai sebanyak –0.573V, 92.95mV/dec, $26.04x10^{-18}$A/μm dan 98.19μA/μm masing-masing. Didalam peranti NMOS, nilai V_{TH}, SS, I_{OFF} dan I_{ON} selepas dioptimumkan adalah +0.546V, 85.08mV/dec, 2.034pA/μm dan 344.17μA/μm masing-masing. Kebanyakan keputusan adalah didalam julat yang dibenarkan dan memenuhi keperluan yang telah ditetapkan oleh teknologi kuasa rendah (LP) untuk tahun 2016 yang telah ditetapkan oleh Hala Tuju Teknologi Antarabangsa bagi Semikonduktor (ITRS) 2013. Sebagai kesimpulan, rekabentuk NMOS and PMOS SOI MOSFET telah berjaya direka dan melalui kaedah Taguchi, penyelesaian optimum untuk reka bentuk yang tegap untuk peranti telah berjaya dicapai.

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LIST OF ABBREVIATION

ANOVA	-	Analysis of Variance
BOX	-	Buried oxide thickness
CMOS	-	Complementary Metal–Oxide Semiconductor
FD MOSFET	-	Full depeleted SOI MOSFET
I_{OFF}	-	Gate leakage current
I_{ON}	-	Drive current
ITRS	-	International Technology Roadmap for Semiconductors
L	-	Channel Length
MOS	-	Metal Oxide Semiconductor
MOSFET	-	Metal Oxide Semiconductor Field Effect Transistor
NMOS	-	N-type MOSFET
OA	-	Orthogonal array
PD MOSFET	-	Partially depleted SOI MOSFET
PMOS	-	P-type MOSFET
S/D	-	Source/Drain
SCE	-	Short channel effect
SOI	-	Silicon-on-insulator
SS	-	Subthreshold swing
TCAD	-	Technology Computer Aided Design
V_{TH}	-	Threshold voltage
VWF	-	Virtual Wafer Fab

LIST OF APPENDICES

LIST OF PUBLICATIONS

The research papers produced and published during the course of this research are as follows:

Journals:

1. Aziz, M.N.I.A., Salehuddin, F., Zain, A.S.M., Kaharudin, K.E. & Radzi, S.A. 2014, "Comparison of electrical characteristics between Bulk MOSFET and Silicon-on-insulator (SOI) MOSFET", Journal of Telecommunication, Electronic and Computer Engineering, vol. 6, no. 2, pp. 45-49.
2. Aziz, M.N.I.A., Salehuddin, F., Zain, A.S.M. & Kaharudin, K.E. 2015, "Study of electrical characteristic for 50nm and 10nm SOI body thickness in MOSFET device", Jurnal Teknologi, vol. 77, no. 21, pp. 109-115.
3. Aziz, M.N.I.A., Salehuddin, F., Zain, A.S.M. & Kaharudin, K.E. 2016, "The consequence of source/drain factor toward drive current in 10nm soi mosfet device", ARPN Journal of Engineering and Applied Sciences, vol. 11, no. 18, pp. 10909-10914.

Conference papers:

1. Aziz, M.N.I.A., Salehuddin, F., Zain, A.S.M., Kaharudin, K.E., Hazura, H., Idris, S.K., Hanim, A.R. & Manap, Z. 2016, "Analyze of threshold voltage in SOI PMOSFET device using Taguchi method", IEEE International Conference on Semiconductor Electronics, Proceedings, ICSE, pp. 97.